What is Claimed is:

[c1] A method of diagnosing a complex semiconductor device utilizing logic circuits, formed of latches, that have failed functional testing comprising the steps of :

combining functional testing of the device circuitry with structural design and test techniques to dynamically create a new test pattern based on the functional failure; and

determining the location of and type of error in the failing circuit.

[c2] The method of claim 1 wherein the step of said combining functional testing of the device circuitry with structural design and test techniques to dynamically create a new test pattern based on the functional failure includes the step of transforming a functional pattern into a scan deterministic pattern.

[c3] The method of claim 2 wherein the device circuitry is stuck at zero.

[c4] The method of claim 2 wherein the device circuitry is stuck at one

[c5] The method of claim 2 wherein the device circuitry has AC faults.

[c6] The method of claim 2 wherein the device circuitry has transitional faults.

[c7] A method of testing a complex semiconductor device utilizing scan chains and logic circuits, formed of latches, consisting of the steps of:

performing a functional test, comprised of a selected number of test cycles, on said semiconductor device;

identifying any failure during the functional test;

unloading the values of the latches from the scan chain before the identified failure may include reading the embedded circuit memories and other circuit storage elements;

generating a Load from the unloaded states of the latches;

applying the generated Load which as the first event of a newly created independent LSSD deterministic pattern using the same identical primary inputs and Clocks that produced the failure to known correctly operating device using the bootstrapping technique and unloading the output of the correctly operating device to generate a deterministic LSSD pattern; and

operating the generated deterministic LSSD pattern to the failing device

and diagnosing the failure using existing LSSD deterministic tools.

[c8] The method of claim 3 wherein said scan chains are LSSD scan chains and said created independent deterministic patterns are LSSD deterministic patterns.

[c9] The method of claim 3 wherein said scan chains are GSD scan chains and said created independent deterministic patterns are GSD deterministic patterns.

[c10] A method of diagnosing a complex semiconductor device utilizing logic circuits, formed of latches, that have failed functional testing comprising the steps of :

identifying a failing vector of the functional test;

observing the states of the failed device by unloading the values of the latches from the LSSD scan chain before the failing vector which may include reading the embedded circuit memories and other circuit storage elements;

generating a LOAD from the unloaded states of the latches:

applying the generated LOAD which as the first event of a newly created independent LSSD deterministic pattern using the same identical primary inputs and Clocks that produced the failure to known correctly operating device using the bootstrapping technique and unloading the output of the correctly operating device to generate a deterministic LSSD pattern; and

operating the generated deterministic LSSD pattern to the failing device and diagnosing the failure using existing LSSD deterministic tools.

[c11] The method of claim 6 wherein said scan chains are GSD scan chains and said created independent deterministic patterns are GSD deterministic patterns.

[c12] A method of diagnosing a complex semiconductor device utilizing logic circuits, formed of latches, that have failed functional testing comprising the steps of :

combining functional testing of the device circuitry with structural design and test techniques to dynamically create new test patterns based on the functional failure; and

determining the location of and type of error in the failing circuit.

[c13] The method of claim 1 wherein the step of said combining functional testing of the device circuitry with structural design and test techniques to dynamically

create new test patterns based on the functional failure includes the step of transforming functional patterns into scan deterministic patterns.

[c14] A testing protocol for determining whether any of the internal functional circuit elements in a complex solid state device is stuck, comprising the steps of:

applying a predetermined set of functional vectors have been applied thus allowing functional patterns to a solid state device;

allowing the set of device run at speed until the failing point is reached;

unloading the data from said device state of the machine; and

isolating the fault.

[c15] The testing protocol of claim 8 wherein the scan access initializes the internal state of the device prior to applying the functional patterns to narrow the partition of the functional patterns; and

iteratively executing multiple partitions to ultimately yield one or more independent scan test vectors.